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5. (Amended) The method as defined in claim 3, wherein a dosage of the arsenic ion is determined to obtain desired electrical characteristics for said semiconductor device, and an acceleration energy and a dosage of the phosphorous ion are determined such that an ion-implanted region of the phosphorous ion extends beyond a bottom surface of an ion-implanted region of the arsenic ion.

B1
C1

Please add the following new claims:

-- 8. A method for manufacturing a semiconductor device comprising:

implanting arsenic ions in a semiconductor substrate at a first acceleration energy level to form an arsenic ion implanted region;

implanting phosphorous ions in said arsenic ion implanted region at a second acceleration energy level lower than said first acceleration energy level; and

heat-treating said ion-implanted regions to activate said arsenic ions and phosphorous ions to form an n-type source/drain main region comprising arsenic and phosphorous ions, and an n-type source/drain buffer region comprising phosphorous ions, said n-type source/drain buffer region extending beyond said n-type source/drain main region.

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B2

9. The method as defined in claim 8, wherein said device comprises an n-type metal oxide semiconductor field effect transistor (NMOSFET).

10. The method as defined in claim 9, wherein said NMOSFET comprises a gate electrode formed over a channel region, and wherein said n-type source/drain buffer region separates said n-type source/drain main region from said channel region.

11. The method as defined in claim 10, wherein said substrate comprises monocrystalline silicon and said arsenic ion implanted region comprises an amorphous silicon region.

12. The method as defined in claim 11, wherein a p-n junction formed at a first interface between said channel region and said buffer region is separated from a second interface

between said amorphous silicon region and said monocrystalline silicon.

13. The method as defined in claim 11, wherein point defects generated by said implanting phosphorous ions are absorbed by said amorphous silicon, such that diffusion of said phosphorous ions during said heat-treating is suppressed.

14. The method as defined in claim 8, wherein said first acceleration energy is reduced without increasing a p-n junction leakage current.

C1
B2

15. The method as defined in claim 8, wherein said first acceleration energy level comprises about 10 keV or less.

16. The method as defined in claim 8, wherein said heat-treating comprises heat treating at about 1000°C for about 10 seconds.

17. The method as defined in claim 8, wherein an arsenic concentration in said n-type source/drain main region is between 1 x 10^{20}/cm^2 and 5 x 10^{21}/cm^2 and a phosphorous concentration in said n-type source/drain buffer region is between 1 x 10^{18}/cm^2 and 5 x 10^{19}/cm^2. - -